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Generalised Approaches for ALU Design Using Reversible Gates

DR. Neelam Rup Prakash[1], Neha Pannu[2]
Department of Electronics and Communication Engineering,
PEC University of Technology, Sector-12, Chandigarh, INDIA.

***Abstract*— Nano-computer designing involves specification of every smallest unit present as well as the covalent bond between them. It is expected that the basic building blocks of the logic elements and even switches and gates are of the order of a nanometer in size. At this scale of magnitude, the use of quantum computing becomes crucial as resorting to erasing great number of bits will hinder the performance of the system. Many researchers try to reduce the use and loss of information bits to a minimum by reusing the outputs as input to some other stage. Basic reversible gates with different set of inputs are used to realize the desired Boolean function. Also, customised MRG and POAG gates are used in novel programmable reversible logic gate structures aimed at design flexibility on different instruction set architectures. ALU is a very important part in every computing system. Proposed designs from various authors including a design using Toffoli gate series and NOT gate along with function generator and DXOR are studied. Another proposal includes the introduction of a YAG gate to simplify implementation of the reversible ALU.**

***Keywords*— Quantum computing, Reversible logic, Function generator, garbage outputs.**

I. INTRODUCTION

According to Moore's law, power dissipation in a computer system gets doubled every few years and we will soon reach the threshold below which transistors will not work because of quantum effects. The heat dissipated due to the production of garbage bits is a major issue. The reversible gates provide a useful alternative to the conventional gates for coping up with this problem. Landaeur has suggested the heat dissipation to be kTln2 Joules for every information bit lost, where k is the Boltzmann's constant and T is the temperature of the system. For the execution of reversible computing, the utilization of energy should be reduced to a bare minimum theoretically. Reversible gates are bijective in the true sense of the word. Also, Benett suggested that the heat dissipation gets reduced to zero by using reversible gates. The design of ALU making use of different reversible gate combinations is studied thoroughly. The key parameters vary with each design trying to make the circuit advantageous in some way. The main focus always relies on reducing the power dissipation.

II. DESIGNING A REVERSIBLE ALU

The base for introducing the concept of quantum gates was provided by Landauer [5] in 1961. It was then that the exact heat loss due to the loss of every individual information bit was given to be kTln2 Joules, where k is the Boltzmann constant and T is the temperature. This result has been very helpful since its advent as the power dissipation is one of the major causes of errors while performing computations. Hence, irreversibility as the only form of performing computations was questioned. This is where quantum computing came into effect.

Benett[1], in 1973, introduced the possibility of zero power dissipation by making use of reversible gates as a replacement for conventional gates for the implementation of our circuits. The computers were proposed in a thermodynamically reversible form.

W. David Pan and Mahesh Nalasani[2] in 2005 introduced the reversible logic gates. The functionality of the basic reversible gates is the foremost factor in the design using reversibility. Some of the commonly used gates function as follows:

1) Controlled NOT Gate/ FREDKIN Gate:
It may also be expressed as (a XOR b).

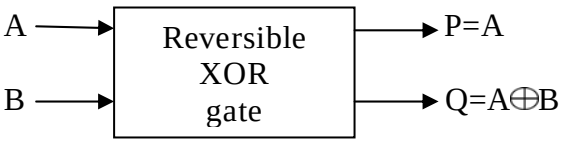

Fig 1. CNOT Gate

The truth table is as follows:

TABLE 1. **TRUTH TABLE FOR CNOT GATE**

INPUTS		OUTPUTS	
A	B	P	Q
0	0	0	0
0	1	0	1
1	0	1	1
1	1	1	0

2) TOFFOLI Gate:
The block diagram provided is self-explanatory.

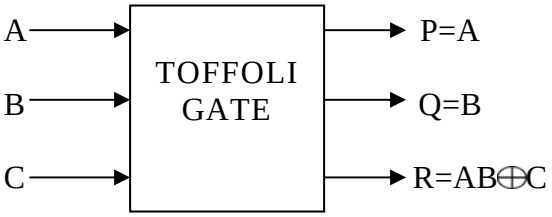

Fig 2. TOFFOLI Gate

3) FREDKIN Gate:

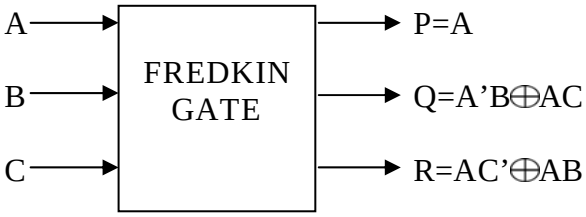

Fig 3. FREDKIN Gate

4) PERES Gate:

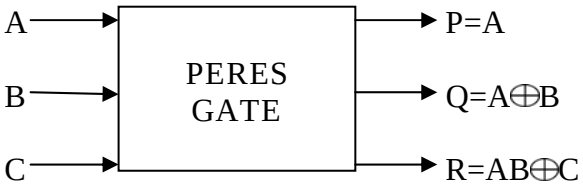

Fig 4. PERES Gate

The fundamental gates having lowest quantum cost of one are the V, V+ and CNOT gates. The cost of any other gates present in the circuit are calculated by counting the number of V, V+ and CNOT gates present in their circuit. The functionality of V is that it provides the square root of NOT gate and V+ gives its Hermitian.

Syamala Y., Tilak A.V.N. [9] have designed a control unit based ALU which makes use of 9n elementary reversible gates for four operations, namely, addition, AND, OR and EXOR. The third input bit is varied in order to realize AND gate, OR gate etc. through Toffoli gate itself. They have also proposed a new programmable logic structure YAG gate for realizing AND and OR functions, as shown in Figure 5.

5) YAG Gate:

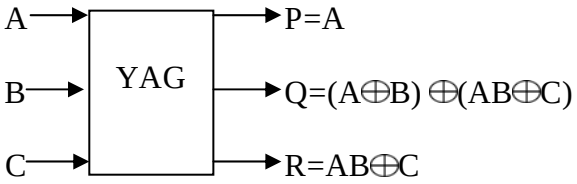

Fig 5. YAG Gate

The quantum execution to calculate the quantum cost through minor units is presented. They have taken into account six factors that ease the reversible circuit design complexity and performance. They are: Gate Count, Garbage outputs, Quantum cost, logical calculation, Quantum depth and constant inputs. The designed ALU makes use of a 4:1 multiplexer for operation selection. It owes its simple implementation to the several independent sub-circuits it is made of. The operations are faster because of the use of parallel logic but everything has its pros and cons. The disadvantage here is a large logic width along with greater number of constant inputs. Two designs are proposed for the suggested ALU: Type I and Type II. Type I uses the conventional gates, nine in number namely 3 Peres, 4 Fredkin and 2 Feynman. Type II uses 7 gates, namely 3 Fredkin, 1 Peres, 1 Feynman, 1 DPG (Double Peres Gate) and 1 YAG. The above-mentioned six parameters are compared and the usage of DPG and YAG gates reduces them. Another reversible ALU based on control structure with a smaller logic width but slower speed is proposed. It is based on both combinational as well as sequential designs(possibly using constant inputs).

Morrison Matthew and Ranganathan Nagarajan[7] have tried the approach of minimizing quantum cost for reducing the computational complexity of the device as well as the time lag and lastly, auxiliary inputs and garbage outputs that only serve the reversibility of the device also need to be minimised. Two gates: MRG and PAOG are proposed and their functionality is verified in Verilog. In comparison to the previous work, design flexibility achieved is higher so that modifications in various Instruction Set Architectures are simpler compared to previous work where significant redesign was needed. Disadvantage is that it incurs two garbage bits per bit whereas the previous work[11] has no garbage bits.

6) MRG Gate:

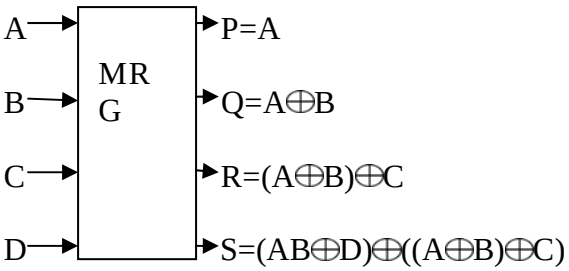

Fig 6. MRG Gate

7)PAOG Gate:

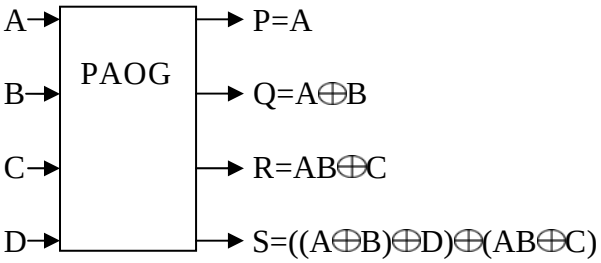

Fig 7. PAOG Gate

Guan Zhijin, Li Wenjuan, Ding Weiping, Hang Yueqin and Ni Lihui[3] proposed that reduction in the temperature of the computer system or constructing a reversible computer on thermodynamics are both effective. The energy consumption gets reduced by two orders of magnitude when the temperature reduces to 0K.The electric charge on the storage cell which consist of transistors remains inside while switching the transistor. That charge can be reused later through reversible operations, which can reduce the energy consumption. They have used Toffoli gate series, NOT gate, swap gate with and without control bit. Fundamental units are function generator and DXOR. The simulation to verify the functionality is done using C++. The use and loss of information bits is significantly reduced which has great relevance to more complex reversible circuits.

Table 2. Comparison Table

PARAMETERS	ALU NAME			
	Morrison Matthew and Ranganathan Nagarajan	**Thomsen M., Gluck R., and Axelsen H.**	**Syamala Y., Tilak A.V.N.**	**Guan Zhijin, Li Wenjuan, Ding Weiping, Hang Yueqin and Ni Lihui**
PROGRAMMABLE LOGIC USED	PAOG, MRG, HNG and Integrated Qubit Gate	Fundamental Gates	YAG, DPG	Fundamental Gates
OPERATIONS PERFORMED	OR, NOR, AND, NAND, ADD, SUB	ADD, SUB, NSUB, EXOR, NOP	ADD, AND, OR, EXOR	16 operations
GATES USED	Peres, Feynman, Toffoli, Fredkin	Feynman, Toffoli, Fredkin	Feynman, Toffoli, Fredkin, Peres	Feynman, Toffoli, Fredkin
ADVANTAGES	Lesser quantum delay, design flexibility, more number of logical calculations	Lower quantum cost, No garbage bits	Simple to design, fast, lesser number of gates using control signal	Reduces information bits loss, reduced cost of circuit design
DISADVANTAGES	2 garbage bits per useful bit		Large logic width, More number of constant inputs	

Premananda B S, Ravindranath Y M[8] have used low-power CMOS technology. But there is restriction on feedback and the fanout is always kept one leading to the presence of garbage bits in output. All the blocks are designed using Verilog and simulated using Cadence NC Sim simulator version 9.10. It has led to 11% power reduction in comparison with conventional 16-bit ALU. However, the number of garbage bits produced is significantly higher.

III. COMPARISON

The table for comparison between the ALUs made by Morrison Matthew and Ranganathan Nagarajan[7], Thomsen M., Gluck R., and Axelsen H[11], Syamala Y., Tilak A.V.N[10], Guan Zhijin, Li Wenjuan, Ding Weiping, Hang Yueqin and Ni Lihui[3] is given on the left side. It provides a clear comparison based on different parametes such as programmable logic used, operations performed, number of gates used and their advantages and disadvantages with respect to other designs.

IV. CONCLUSIONS

The reversible ALU design is a very low-energy dissipation circuit. The information loss bits can be reduced using various methods and varying the gates used to implement a particular function. Other than the fundamental quantum gates available, customised gates can also be used whose functionality can be chosen and by varying the inputs given, they can be used to perform several functions. The most optimum circuit uses minimum constant inputs. Also, function generator or multiplexer or control unit can be used for choosing the operation of our choice that the ALU needs to carry out.

The design can be checked using various online or commercially available simulators. SPICE simulations of reversible circuits have shown that such implementations have the potential to reduce energy consumption by a factor of 10[6]. Tthere is a lot of scope in this area for research as well as finding out other possible methods for implementation and synthesis of reversible logic circuits.

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